Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Original) A hierarchical test control network for an integrated circuit, comprising:

a top-level test control circuit block, said top-level test control circuit block comprising a chip access port (CAP) controller; and

a plurality of lower-level test control circuit blocks connected to said top-level test control circuit block in a hierarchical structure, each of said lower-level test control circuit blocks comprising a socket access port (SAP) controller;

wherein test operation is transferred downward and upwards within said hierarchical structure.

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2 – 14 (Canceled)

15. (New) The hierarchical test control network of claim 1, wherein the lower-level test control circuit blocks are connected in a serial chain.

16. (New) The hierarchical test control network of claim 1, wherein each of said lower-level test control circuit blocks is connected to a different virtual circuit block for controlling testing thereof.

17. (New) The hierarchical test control network of claim 1, wherein each of said lower-level test control circuit blocks comprises a test mode select input port, a test data input port, and a test data output port.

18. (New) The hierarchical test control network of claim 1, wherein said top-level test control circuit block and said plurality of lower-level test control circuit blocks are organized in a plurality of tiers.

19. (New) The hierarchical test control network of claim 18, wherein all of the lower-level test control circuit blocks connected at a same tier collectively output a common test mode data output signal comprising a logical OR of individual test mode data output signals output from each of the lower-level test control circuit blocks connected at the same tier.

20. (New) A hierarchical test control network for an integrated circuit, comprising:

means for controlling a chip access port (CAP) of a top-level test control circuit block;

means for controlling a plurality of socket access ports (SAPs) for a plurality of lower-level test control circuit blocks, each lower-level test control circuit block connected to said top-level test control circuit block in a hierarchical structure; and

means for transferring test operation downward and upwards within said hierarchical structure.

21. (New) The hierarchical test control network of claim 20, wherein the lower-level test control circuit blocks are connected in a serial chain.

22. (New) The hierarchical test control network of claim 20, wherein each of said lower-level test control circuit blocks is connected to a different virtual circuit block for controlling testing thereof.

23. (New) The hierarchical test control network of claim 20, wherein each of said lower-level test control circuit blocks comprises a test mode select input port, a test data input port, and a test data output port.

24. (New) A method of testing a plurality of virtual circuit blocks of an integrated circuit, comprising:

transferring test vectors from an access port of the integrated circuit directly to the plurality of virtual circuit blocks;

applying the test vectors to a scan chain of each virtual circuit block;

capturing test responses of each scan chain; and

transferring the captured test responses from the plurality of virtual circuit blocks directly to the access port of the integrated circuit.

25. (New) The method of claim 24, wherein at least one of the plurality of virtual circuit blocks comprises a foundation virtual circuit block with a plurality of internal virtual circuit blocks, the method further comprising:

transferring the test vectors from the foundation virtual circuit block to the plurality of internal virtual circuit blocks.

26. (New) The method of claim 25, further comprising:

controlling a test of one or more of the internal virtual circuit blocks directly through the access port of the integrated circuit.

27. (New) The method of claim 25, wherein the foundation virtual circuit block comprises a system on a chip, wherein a first internal virtual circuit block comprises a microprocessing device, and wherein a second internal virtual circuit block comprises a memory device.

28. (New) The method of claim 27 further comprising:

transferring a microprocessor test pattern from the access port of the integrated circuit to the microprocessing device; and

transferring a memory test pattern from the access port of the integrated circuit to the memory device.

29. (New) The method of claim 25, wherein at least one of the virtual circuit blocks comprises a peripheral circuit block.

30. (New) The method of claim 24, further comprising:

individually accessing each of the plurality of virtual circuit blocks through the one or more pins of the integrated circuit.